



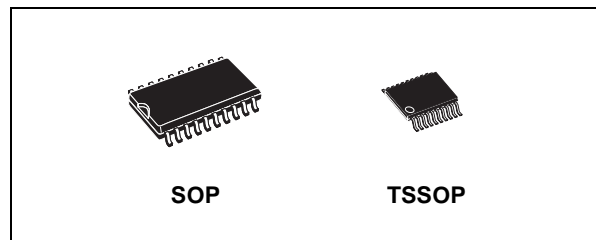
74LVQ299

8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

- HIGH SPEED:
 $t_{PD} = 8.3 \text{ ns}$ (TYP.) at $V_{CC} = 3.3 \text{ V}$
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- LOW NOISE:
 $V_{OLP} = 0.5\text{V}$ (TYP.) at $V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 12\text{mA}$ (MIN) at $V_{CC} = 3.0 \text{ V}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2\text{V}$ to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74LVQ299 is a low voltage CMOS 8 BIT PIPO SHIFT REGISTER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power and low noise 3.3V applications.



ORDER CODES

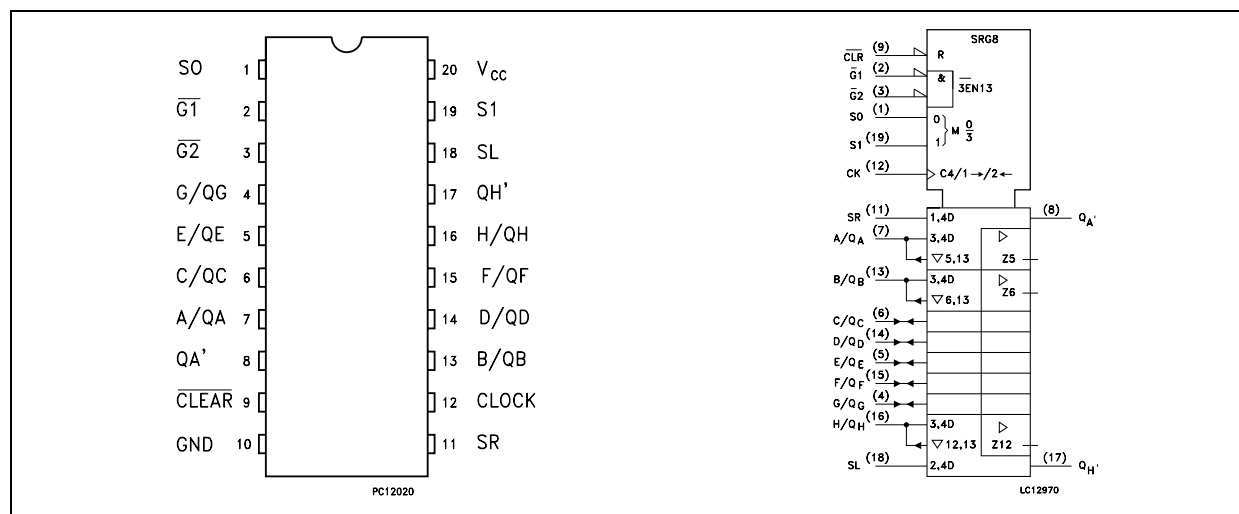
| PACKAGE | TUBE | T & R |
|---------|-----------|-------------|
| SOP | 74LVQ299M | 74LVQ299MTR |
| TSSOP | | 74LVQ299TTR |

These devices have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1) as shown in the Truth Table.

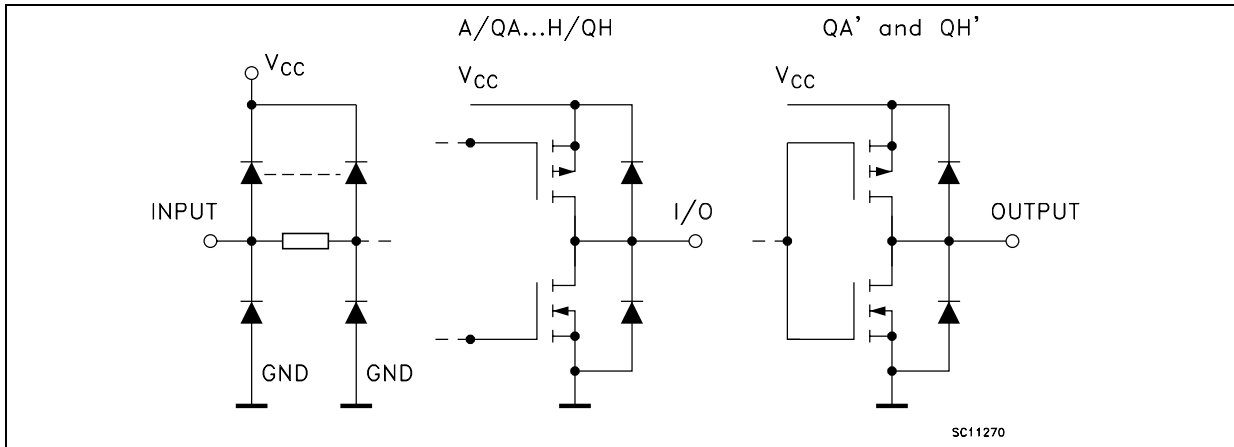
When one or both enable inputs, $\overline{G1}$, $\overline{G2}$ are high, the eight input/output terminals are in the high impedance state; however sequential operation or clearing of the register is not affected. Clear function is asynchronous to clock.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

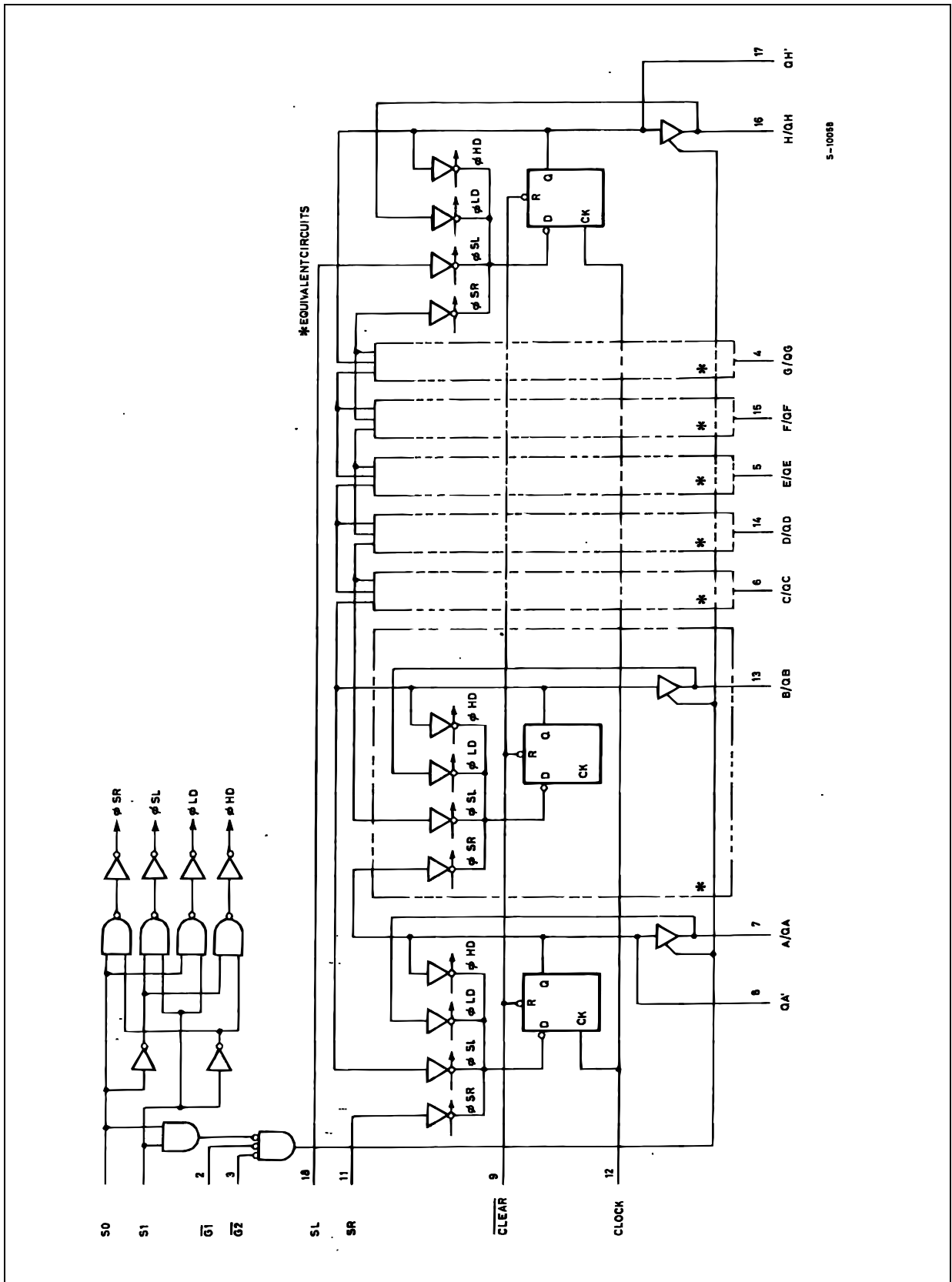
| PIN No | SYMBOL | NAME AND FUNCTION |
|----------------------------|-----------------|---|
| 1, 19 | S0, S1 | Mode Select Inputs |
| 2, 3 | G1, G2 | 3-State Output Enable Inputs (Active LOW) |
| 7, 13, 6, 14, 5, 15, 4, 16 | A/QA to H/QH | Parallel Data Inputs or 3-State Parallel Outputs (Bus Driver) |
| 8, 17 | QA',QH' | Serial Outputs (Standard Output) |
| 9 | CLEAR | Asynchronous Master Reset Input (Active LOW) |
| 11 | SR | Serial Data Shift Right Input |
| 12 | CLOCK | Clock Input (LOW to HIGH, Edge-triggered) |
| 18 | SL | Serial Data Shift Left Input |
| 10 | GND | Ground (0V) |
| 20 | V _{CC} | Positive Supply Voltage |

TRUTH TABLE

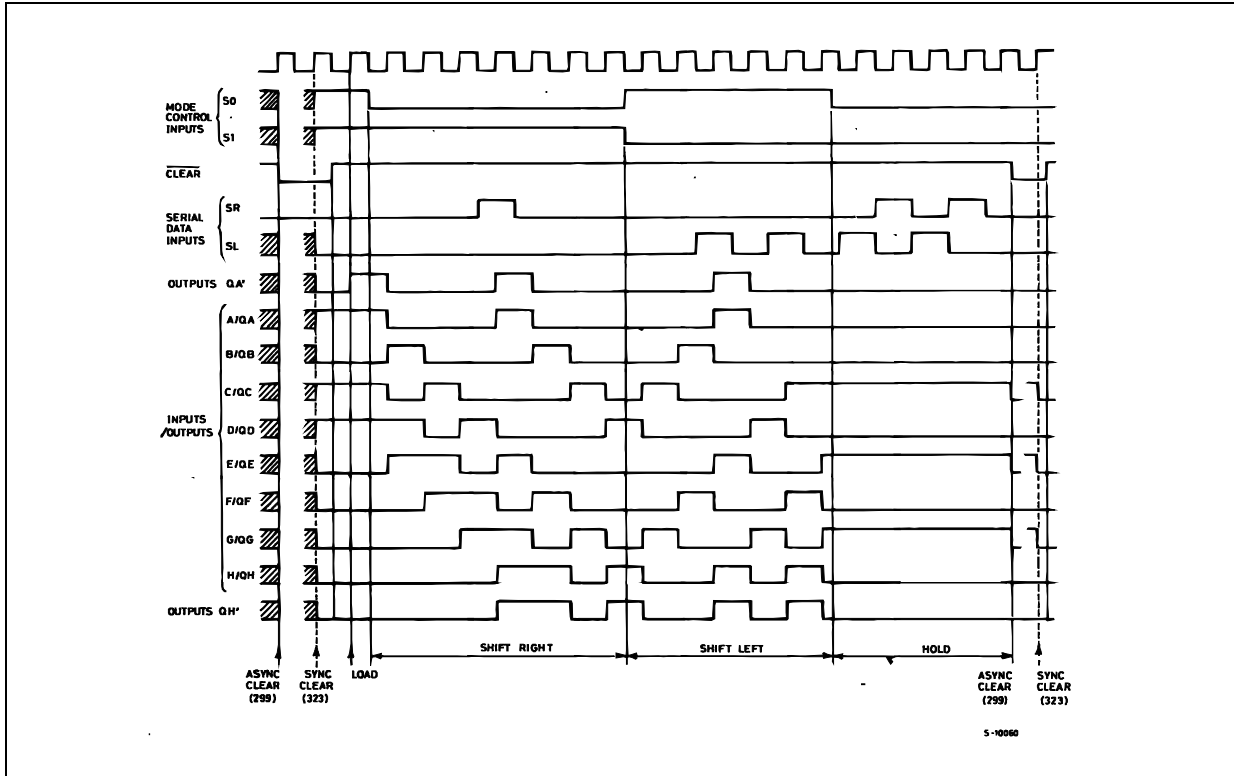
| MODE | INPUTS | | | | | | INPUTS/OUTPUTS | | | | OUTPUTS | |
|-------------|--------|-------------------|----|----------------|-----|-------|----------------|----|------|------|---------|-----|
| | CLEAR | FUNCTION SELECTED | | OUTPUT CONTROL | | CLOCK | SERIAL | | A/QA | H/QH | QA' | QH' |
| | | S1 | S0 | G1* | G2* | | SL | SR | | | | |
| Z | L | H | H | X | X | X | X | X | Z | Z | L | L |
| CLEAR | L | L | X | L | L | X | X | X | L | L | L | L |
| | L | X | L | L | L | X | X | X | L | L | L | L |
| HOLD | H | L | L | L | L | X | X | X | QA0 | QH0 | QA0 | QH0 |
| SHIFT RIGHT | H | L | H | L | L | ┌ | X | H | H | QGn | H | QGn |
| | H | L | H | L | L | └ | X | L | L | QGn | L | QGn |
| SHIFT LEFT | H | H | L | L | L | ┌ | H | X | QBn | H | QBn | H |
| | H | H | L | L | L | └ | L | X | QBn | L | QBn | L |
| LOAD | H | H | H | X | X | ┌ | X | X | a | h | a | h |

* When one or both controls are high, the eight input/output terminals are the high impedance state: however sequential operation or cleaning of the register is not affected.
 Z : High Impedance
 Qn0 : The level of An before the indicated steady state input conditions were established.
 Qnn : The level of Qn before the most recent active transition indicated by OR
 a, h : The level of the steady state inputs A, H, respectively.
 X : Don't Care

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|-------------------------------|------------------------|-------------|
| V_{CC} | Supply Voltage | -0.5 to +7 | V |
| V_I | DC Input Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | DC Input Diode Current | ± 20 | mA |
| I_{OK} | DC Output Diode Current | ± 20 | mA |
| I_O | DC Output Current | ± 50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 400 | mA |
| T_{stg} | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (10 sec) | 300 | $^{\circ}C$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|----------|---|---------------|-------------|
| V_{CC} | Supply Voltage (note 1) | 2 to 3.6 | V |
| V_I | Input Voltage | 0 to V_{CC} | V |
| V_O | Output Voltage | 0 to V_{CC} | V |
| T_{op} | Operating Temperature | -55 to 125 | $^{\circ}C$ |
| dt/dv | Input Rise and Fall Time $V_{CC} = 3.0V$ (note 2) | 0 to 10 | ns/V |

1) Truth Table guaranteed: 1.2V to 3.6V
 2) V_{IN} from 0.8V to 2V



DC SPECIFICATIONS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|------------------|---------------------------------------|------------------------|--|-----------------------|-------|-------|-------------|-------|--------------|-------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{IH} | High Level Input Voltage | 3.0 to 3.6 | | 2.0 | | | 2.0 | | 2.0 | | V |
| V _{IL} | Low Level Input Voltage | | | | | 0.8 | | 0.8 | | 0.8 | V |
| V _{OH} | High Level Output Voltage | 3.0 | I _O =-50 μA | 2.9 | 2.99 | | 2.9 | | 2.9 | | V |
| | | | I _O =-12 mA | 2.58 | | | 2.48 | | 2.48 | | |
| | | | I _O =-24 mA | | | | 2.2 | | 2.2 | | |
| V _{OL} | Low Level Output Voltage | 3.0 | I _O =50 μA | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | I _O =12 mA | | 0 | 0.36 | | 0.44 | | 0.44 | |
| | | | I _O =24 mA | | | | | 0.55 | | 0.55 | |
| I _I | Input Leakage Current | 3.6 | V _I = V _{CC} or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I _{OZ} | High Impedance Output Leakage Current | 3.6 | V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND | | | ±0.25 | | ± 2.5 | | ± 5.0 | μA |
| I _{CC} | Quiescent Supply Current | 3.6 | V _I = V _{CC} or GND | | | 4 | | 40 | | 40 | μA |
| I _{OLD} | Dynamic Output Current (note 1, 2) | 3.6 | V _{OLD} = 0.8 V max | | | | 36 | | 25 | | mA |
| I _{OHD} | | | V _{OHD} = 2 V min | | | | -25 | | -25 | | mA |

1) Maximum test duration 2ms, one output loaded at a time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|------------------|--|------------------------|------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V _{OLP} | Dynamic Low Voltage Quiet Output (note 1, 2) | 3.3 | C _L = 50 pF | | 0.5 | 0.8 | | | | | V |
| V _{OLV} | | | | -0.8 | -0.6 | | | | | | |
| V _{IHD} | Dynamic High Voltage Input (note 1, 3) | 3.3 | | 2 | | | | | | | V |
| V _{ILD} | Dynamic Low Voltage Input (note 1, 3) | 3.3 | | | | 0.8 | | | | | V |

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \text{ } \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|--------------------------|--|-----------------|--|--------------------------|------|------|------------------------------------|------|-------------------------------------|------|------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | $-40 \text{ to } 85^\circ\text{C}$ | | $-55 \text{ to } 125^\circ\text{C}$ | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t_{PLH} t_{PHL} | Propagation Delay Time CLOCK to Q'_A or Q'_H | 2.7 | | | 9.7 | 15.0 | | 17.5 | | 20.0 | ns |
| | | 3.3(*) | | | 8.2 | 12.0 | | 14.0 | | 16.5 | |
| t_{PLH} t_{PHL} | Propagation Delay Time CLOCK to A/QA, H/QH | 2.7 | | | 9.8 | 15.0 | | 17.5 | | 20.0 | ns |
| | | 3.3(*) | | | 8.3 | 12.0 | | 14.0 | | 16.5 | |
| t_{PHL} | Propagation Delay Time CLEAR to Q'_A or Q'_H | 2.7 | | | 8.4 | 14.0 | | 16.5 | | 19.0 | ns |
| | | 3.3(*) | | | 7.1 | 11.0 | | 13.0 | | 15.0 | |
| t_{PHL} | Propagation Delay Time CLEAR to A/QA, H/QH | 2.7 | | | 8.9 | 15.0 | | 17.5 | | 20.0 | ns |
| | | 3.3(*) | | | 7.4 | 12.0 | | 14.0 | | 16.5 | |
| t_{PZL} t_{PZH} | Output Enable Time G1 or G2 to A/QA, H/QH | 2.7 | | | 9.9 | 15.0 | | 17.5 | | 20.0 | ns |
| | | 3.3(*) | | | 8.0 | 12.0 | | 14.0 | | 16.5 | |
| t_{PLZ} t_{PHZ} | Output Disable Time G1 or G2 to A/QA, H/QH | 2.7 | | | 9.8 | 15.0 | | 17.5 | | 20.0 | ns |
| | | 3.3(*) | | | 8.0 | 12.0 | | 14.0 | | 16.5 | |
| t_W | CLEAR Pulse Width LOW | 2.7 | | 5.0 | 2.1 | | 5.0 | | 5.0 | | ns |
| | | 3.3(*) | | 4.0 | 2.0 | | 4.0 | | 4.0 | | |
| t_W | CLOCK Pulse Width LOW | 2.7 | | 5.0 | 2.1 | | 5.0 | | 5.0 | | ns |
| | | 3.3(*) | | 4.0 | 2.0 | | 4.0 | | 4.0 | | |
| t_s | Setup Time HIGH or LOW (A/QA, H/ QH to CLOCK) | 2.7 | | 4.0 | 1.4 | | 4.0 | | 4.0 | | ns |
| | | 3.3(*) | | 3.0 | 1.1 | | 3.0 | | 3.0 | | |
| t_h | Hold Time HIGH or LOW (A/QA, H/QH to CLOCK) | 2.7 | | 1.0 | -1.3 | | 1.0 | | 1.0 | | ns |
| | | 3.3(*) | | 1.0 | -1.0 | | 1.0 | | 1.0 | | |
| t_s | Setup Time HIGH or LOW (S0 or S1 to CLOCK) | 2.7 | | 6.0 | 3.1 | | 6.0 | | 6.0 | | ns |
| | | 3.3(*) | | 5.0 | 2.5 | | 5.0 | | 5.0 | | |
| t_h | Hold Time HIGH or LOW (S0 or S1 to CLOCK) | 2.7 | | 1.0 | -3.1 | | 1.0 | | 1.0 | | ns |
| | | 3.3(*) | | 1.0 | -2.6 | | 1.0 | | 1.0 | | |
| t_s | Setup Time HIGH or LOW (SR or SL to CLOCK) | 2.7 | | 4.0 | 1.5 | | 4.0 | | 4.0 | | ns |
| | | 3.3(*) | | 3.0 | 1.1 | | 3.0 | | 3.0 | | |
| t_h | Hold Time HIGH or LOW (SR or SL to CLOCK) | 2.7 | | 1.0 | -1.5 | | 1.0 | | 1.0 | | ns |
| | | 3.3(*) | | 1.0 | -1.1 | | 1.0 | | 1.0 | | |
| t_{REM} | Recovery Time CLEAR to CLOCK | 2.7 | | 1.0 | -0.7 | | 1.0 | | 1.0 | | ns |
| | | 3.3(*) | | 1.0 | -0.5 | | 1.0 | | 1.0 | | |
| f_{MAX} | Maximum Clock Frequency | 2.7 | | 100 | 150 | | 80 | | 60 | | ns |
| | | 3.3(*) | | 120 | 180 | | 100 | | 80 | | |
| t_{OSLH} t_{OSHL} | Output To Output Skew Time (note1, 2) | 2.7 | | | 0.5 | 1.0 | | 1.0 | | 1.0 | ns |
| | | 3.3(*) | | | 0.5 | 1.0 | | 1.0 | | 1.0 | |

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

2) Parameter guaranteed by design

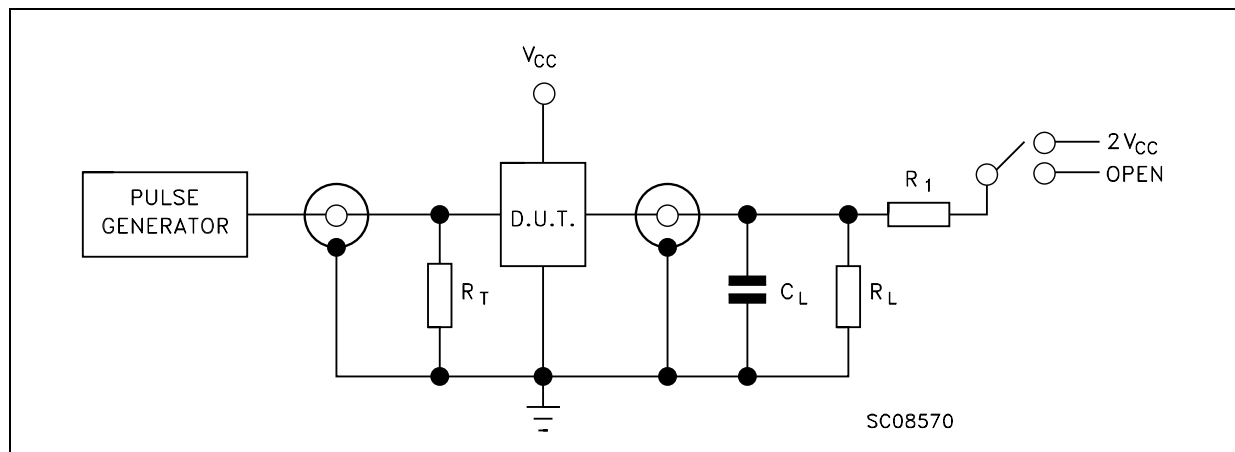
(*) Voltage range is $3.3V \pm 0.3V$

CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|------------------|--|------------------------|-------------------------|-----------------------|------|------|-------------|------|--------------|------|------|
| | | V _{CC} (V) | | T _A = 25°C | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C _{IN} | Input Capacitance | 3.3 | | | 4 | | | | | | pF |
| C _{I/O} | Bus Input Capacitance | | | | | | | | | | pF |
| C _{PD} | Power Dissipation Capacitance (note 1) | 3.3 | f _{IN} = 10MHz | | 10 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

TEST CIRCUIT



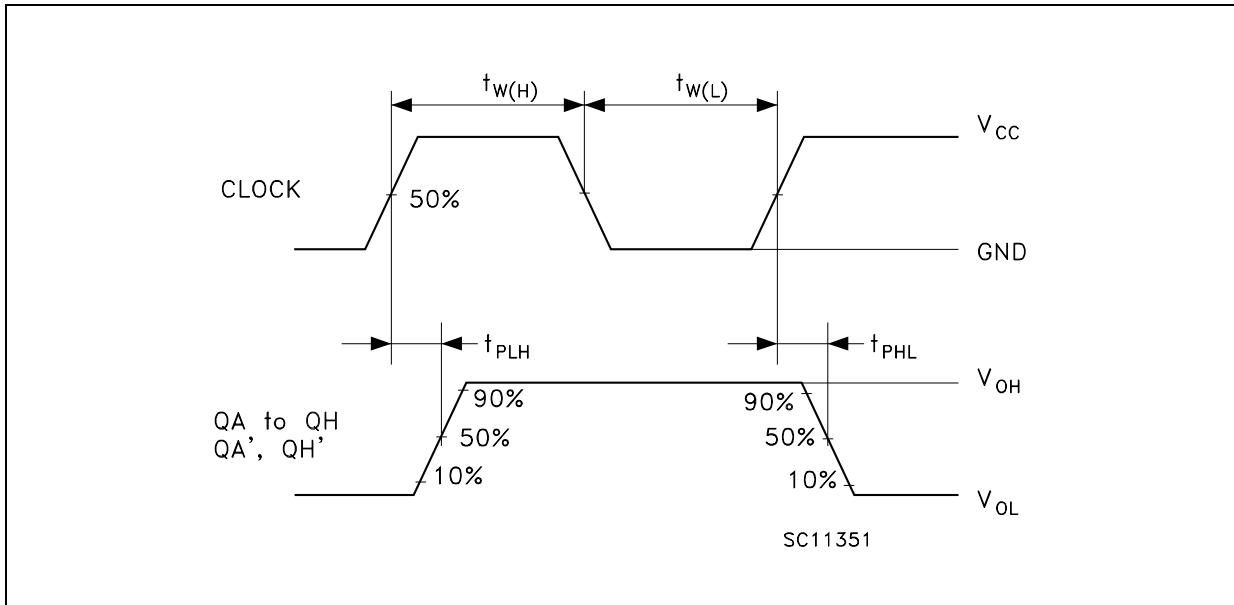
| TEST | SWITCH |
|-------------------------------------|------------------|
| t _{PLH} , t _{PHL} | Open |
| t _{PZL} , t _{PLZ} | 2V _{CC} |
| t _{PZH} , t _{PHZ} | Open |

C_L = 50pF or equivalent (includes jig and probe capacitance)

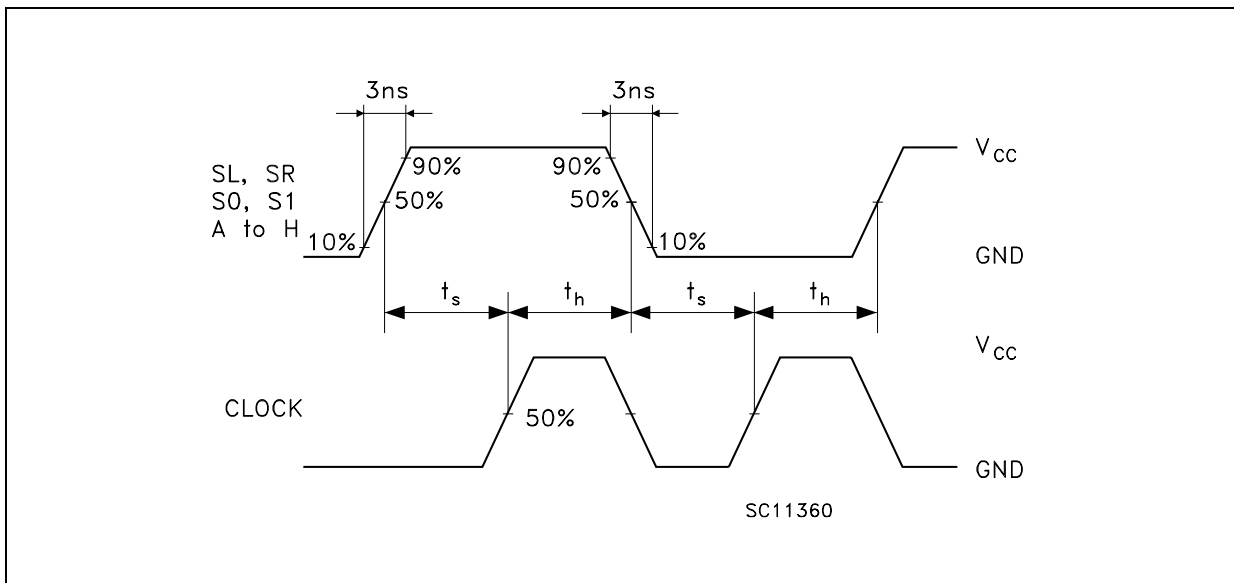
R_L = R₁ = 500Ω or equivalent

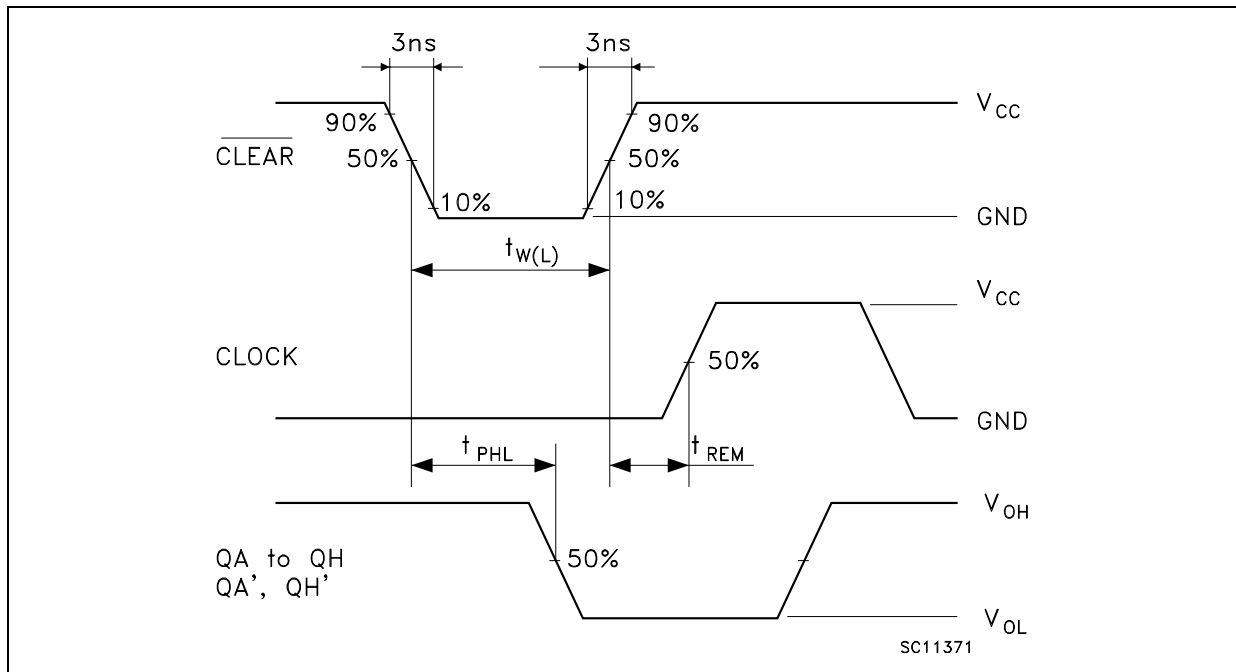
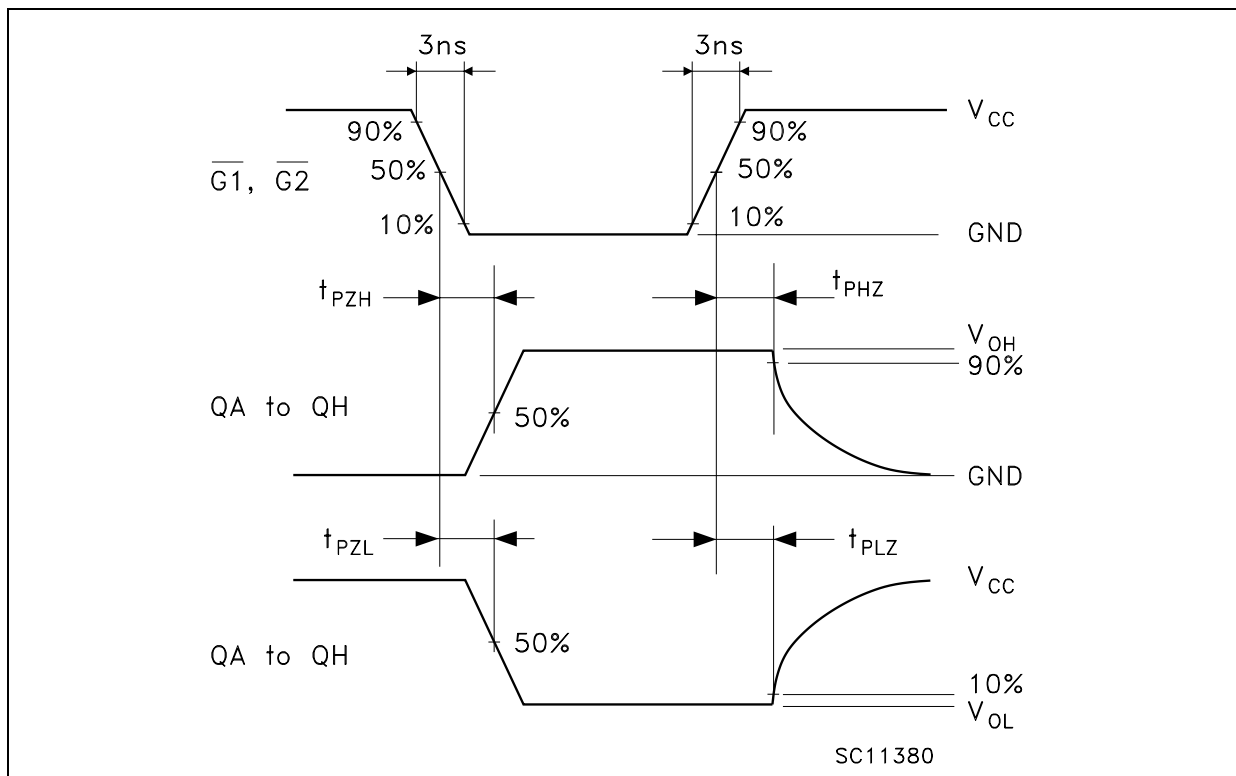
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



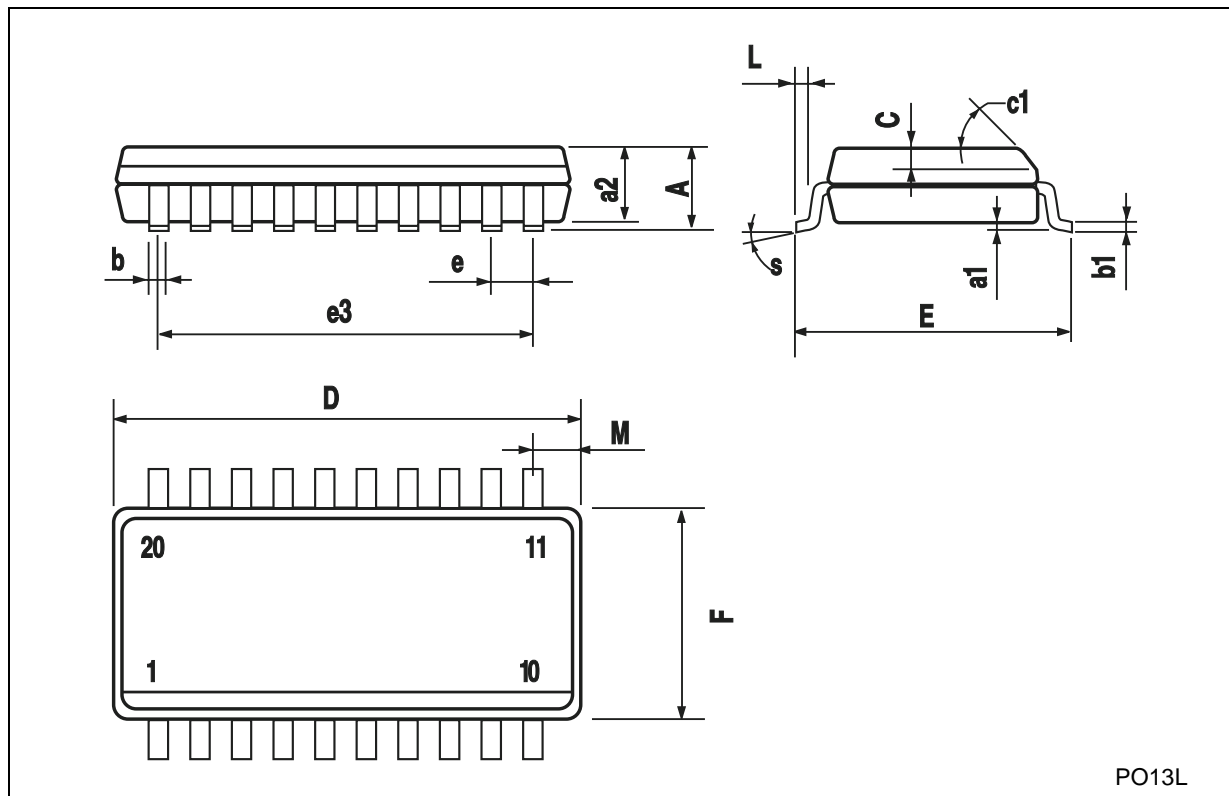
WAVEFORM 2 : PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3 : PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 4 : PROPAGATION DELAYS** ($f=1\text{MHz}$; 50% duty cycle)

SO-20 MECHANICAL DATA

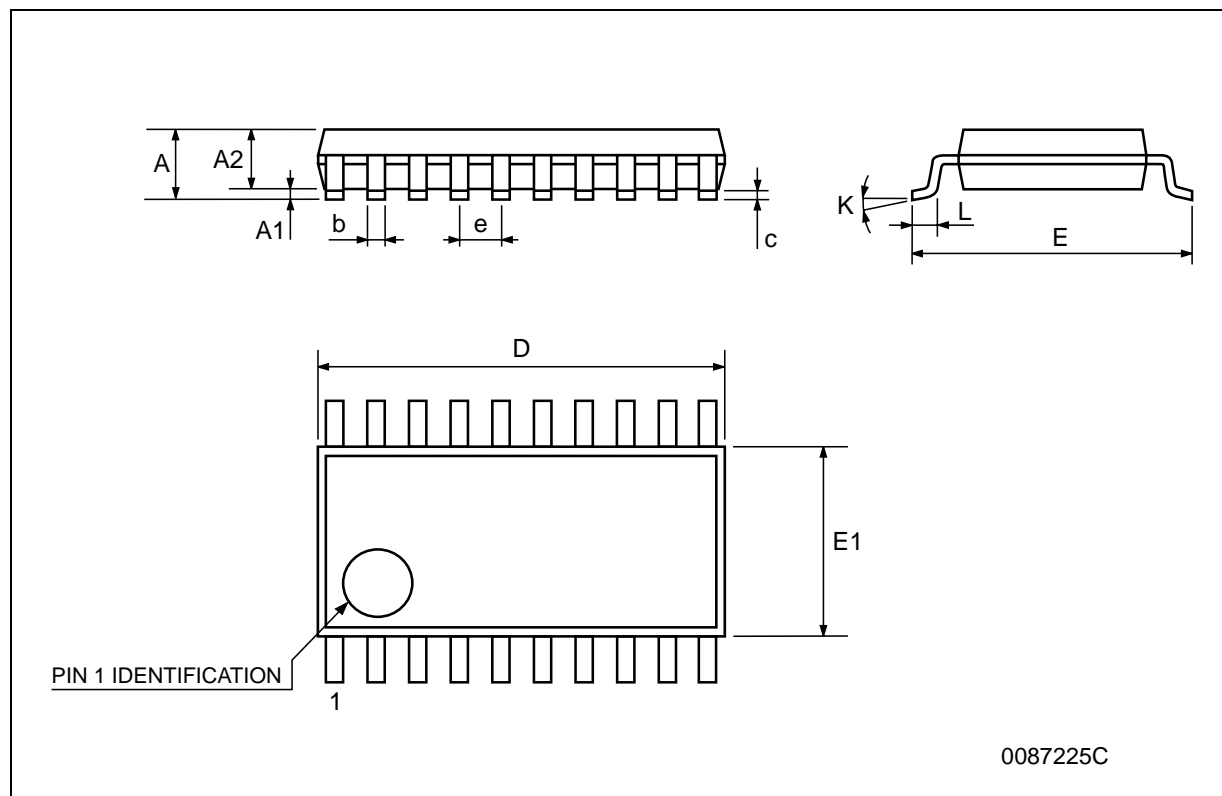
| DIM. | mm. | | | inch | | |
|------|------------|-------|-------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.008 |
| a2 | | | 2.45 | | | 0.096 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.012 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 12.60 | | 13.00 | 0.496 | | 0.512 |
| E | 10.00 | | 10.65 | 0.393 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 11.43 | | | 0.450 | |
| F | 7.40 | | 7.60 | 0.291 | | 0.300 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| M | | | 0.75 | | | 0.029 |
| S | 8° (max.) | | | | | |



PO13L

TSSOP20 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|----------|------|-------|------------|--------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0089 |
| D | 6.4 | 6.5 | 6.6 | 0.252 | 0.256 | 0.260 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



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